a current adjustment transistor coupled to the sources of the first and second transistors, a third gate of the current adjustment transistor receiving the differential output signal of the differential circuit, wherein the current adjustment transistor turns ON and OFF in response to the logic level of the differential output signal.--

REMARKS

The Office Action dated April 15, 2002, has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. By this amendment, claim 1 has been further amended to more clearly set forth the claimed invention. Claim 21 is newly added. No new matter has been added. Accordingly, claims 1, 2 and 4-20 are pending in this application and are submitted for consideration.

Applicant acknowledges and thanks the Examiner for indicating that claims 6-15 are allowed over the prior art.

Claims 1, 2, 4, 5 and 16-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Danstrom [1](U.S. Patent No. 5,801,553) in view of Volk et al. (U.S. Patent No. 5,999,020, "Volk")[2]. The Office Action took the position that Danstrom discloses all the limitations of the claimed invention, except for disclosing that the transistors are FETs. Volk is cited for teaching this limitation. However, Applicant respectfully submits that the prior art, either alone or in combination, fails to disclose or suggest the subject matter of the claimed invention.

[1] The Office Action inadvertently refers to this reference as Danstron.

Claim 1 recites an input circuit comprising a current mirror circuit including a self-biased transistor and a non-self-biased transistor connected to each other, and a differential circuit including a first transistor a first drain of which is connected to the non-self-biased transistor for receiving an external signal and a second transistor a second drain of which is connected to the self-biased transistor for receiving a reference signal. A first source of the first transistor and a second source of the second transistor are connected in common and have the same potential, and the differential circuit generates an internal signal at the first drain in accordance with a current flowing through the first and second transistors. The input circuit further comprises a constant current source connected to the first source of the first transistor, and a current regulating circuit connected to the second source of the second transistor and connected in parallel to the constant current source. The current regulating circuit increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit.

Accordingly, the present invention provides input circuits which amplify external signals to generate internal signals having predetermined amplitudes. Furthermore, as the present invention provides the benefit of having an input circuit generating internal input signals which rise and fall in response to the rising edges and the falling edges of an external input signal.

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[2] The rejection is somewhat unclear. Although the rejection is stated initially to be a 102 rejection, the Examiner states that Danstom is anticipated in view of Volk and concludes with an obviousness rejection type statement. Therefore, Applicant assumes that this is a rejection under 35 U.S.C § 103(a).

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicant's invention, and therefore fails to provide the advantages which are provided by the present invention.

The present invention of is directed to an input circuit that includes a current regulating circuit responsive to an internal signal generated by a differential circuit. The current regulating circuit is connected to the sources of the first and second transistors of the differential circuit and is connected in parallel to the constant current source.

Danstrom is directed to a comparator (58) which includes a current mirror circuit (84, 82), a differential circuit (76, 80), a constant current source (60), hysteresis circuit (62), and an output stage (64) (See Fig. 3).

However, the differential circuit of the present invention is different from that of Danstrom. That is, the emitters of the transistors (76, 80) of the differential circuit of Danstrom are connected via a hysteresis resistor (78). The hysteresis resistor (78) is provided to differentiate emitter voltages of the transistors (76, 80), thereby obtaining the hysteresis characteristics. In contrast, in the present invention, the sources of the transistors of the differential circuit are connected in common and have the same potential, as recited in claim 1.

The Office Action asserted that it would have been obvious to one of ordinary skill in the art to employ the FETs of Volk in the circuit of Danstrom for the purpose of reducing power consumption. However, even if the FETs of Volk are utilized in the circuit of Danstrom, the combination would still fail to disclose or suggest the presently claimed invention, because the Danstrom fails to disclose or suggest that the sources of

the transistors of the differential circuit are connected in common and have the same potential.

Furthermore, claim 16 recites that the source of the first transistor is connected to the source of the second transistor at a first node. Claim 16 also recites a first inverter having an input terminal connected to a second node between the first and fifth transistors. Neither Danstrom nor Volk disclose or suggest these limitations.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 1 and 16 is not obvious within the meaning of 35 U.S.C. § 103.

As claims 2, 4, 5 and 17-20 depend directly or indirectly from claims 1 and 16, respectively, Applicants respectfully submit that each of these claims incorporate the patentable aspects thereof, and are therefore allowable for at least same reasons as discussed above.

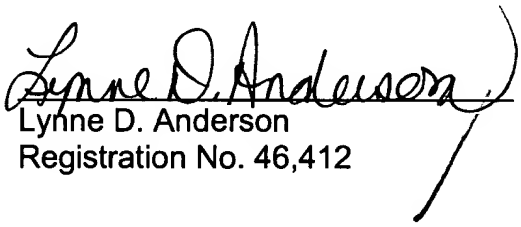
Newly added claim 21 is directed to a data strobe signal input circuit that includes a differential circuit, a current mirror circuit, a constant current source, and a current adjustment transistor. Therefore, it is respectfully submitted that this claim is also patentable over the cited prior art.

In view of the above, Applicant respectfully submits that claims 1, 2, 4, 5 and 16-21, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully requests that claims 1, 2, 4, 5 and 16-21 be found allowable, and that this application be passed to issue along with allowed claims 6-15.

If for any reason the Examiner determines that this application is not now in condition for allowance, it is respectfully requested that the Examiner contact by telephone the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to Counsel's Deposit Account No. 01-2300, **referencing Docket Number 108075-09014.**

Respectfully submitted,



Lynne D. Anderson
Registration No. 46,412

Customer No. 004372
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W., Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6435
Fax: (202) 638-4810

Enclosures: Marked-Up Version of Original Claims
Associate Power of Attorney

MARKED-UP COPY OF ORIGINAL CLAIM 1

1. (Four Times Amended) An input circuit comprising:

a current mirror circuit including a self-biased transistor and a non-self-biased transistor connected to each other;

a differential circuit including a first transistor a first drain of which is connected to the non-self-biased transistor for receiving an external signal and a second transistor a second drain of which is connected to the self-biased transistor for receiving a reference signal, wherein a first source of the first transistor and a second source of the second transistor are connected in common and have the same potential, and the differential circuit generates an internal signal at the first drain in accordance with a current flowing through the first and second transistors;

a constant current source connected to the first source of the first transistor; and

a current regulating circuit connected to the second source of the second transistor and connected in parallel to the constant current source, wherein the current regulating circuit increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit.